RBUS 1305-1

In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A signal interface, comprising:

a set of signal lines having N+1 signal lines, where N is an integer;

N+1 receivers coupled to respective signal lines in the set of signal lines establishing a set of N+1 signal paths with the set of signal lines;

an N line bus;

a line maintenance circuit; and

a switch in the N+1 signal paths, and control logic for the switch, which selectively routes N signal paths in the set to the N line bus and signal path (n) in the set to the line maintenance circuit, where (n) is changed according to a pattern to selectively maintain signal paths in the set of N+1 signal paths while enabling data flow on N signal paths in the set to the N line bus; wherein for a change of (n) by switching a first particular signal path from routing to the line maintenance circuit to routing to a line in the N line bus, and a second particular signal path from routing to the line in the N line bus to the line maintenance circuit, the control logic controls the switch so that reception of data from the line in the N line bus is uninterrupted.

2. (Original) The signal interface of claim 1, wherein the pattern comprises a periodic pattern.

3. (Original) The signal interface of claim 1, wherein the set of N+1 signal paths includes signal paths logically identified as paths 0 to N, and the pattern comprises a repeating pattern beginning with (n) equal to 0 and increasing to (n) equal to N, and then decreasing to (n) equal to 0.

4. (Original) The signal interface of claim 1, wherein the receivers are responsive to respective receive clock signals produced by adjustable clock generators, and said line maintenance circuits set the adjustable clock generators.

5. (Original) The signal interface of claim 1, wherein the receivers are responsive to respective receive clock signals produced by adjustable clock generators, and said line maintenance circuit sets the adjustable clock generators in response to a calibration data pattern on the signal path coupled to the line maintenance circuit.

6. (Currently Amended) A signal interface, comprising:

a set of signal lines having N+1 signal lines, where N is an integer;

N+1 receivers coupled to respective signal lines in the set of signal lines establishing a set of N+1 signal paths with the set of signal lines;

an N line bus;

a line maintenance circuit; and

a switch in the N+1 signal paths, and control logic for the switch, which selectively routes N signal paths in the set to the N line bus and signal path (n) in the set to the line maintenance circuit, where (n) is changed according to a pattern to selectively maintain signal paths in the set of N+1 signal paths while enabling data flow on N signal paths in the set to the N line bus ~~The signal interface of claim~~ 1, wherein ~~the control logic controls the switch~~ for a change of (n) by switching a first particular signal path from routing to the line maintenance circuit to routing to a line in the N line bus, and a second particular signal path from routing to the line in the N line bus to the line maintenance circuit, the control logic controls the switch so that during a settling interval, the first and second particular signal paths both carry data from ~~are routed together to~~ the line in the N line bus, and then after the settling interval the second particular signal path is coupled to the line maintenance circuit.

7. (Original) The signal interface of claim 1, wherein the control logic includes logic for coordinating the pattern with a source of data for the N line bus.

8. (Original) The signal interface of claim 1, wherein said N+1 receivers, said N line bus, said line maintenance circuit; and said switch comprise components of a single integrated circuit.

9. (Original) The signal interface of claim 1, including logic to power down the N+1 receivers while continuing to selectively maintain signal paths in the set of signal paths.

10. (Original) The signal interface of claim 1, wherein the N+1 receivers are adapted to receive data with a data rate higher than 100 MegaHertz.

11. (Original) The signal interface of claim 1, wherein said N+1 receivers, said N line bus, said line maintenance circuit; and said switch comprise components of a single integrated circuit, and the N+1 receivers are adapted to receive data with a data rate higher than 100 MegaHertz from a source external to the integrated circuit.

12. (Original) The signal interface of claim 1, further including an additional signal line adapted to receive a source synchronous clock.

13. (Currently Amended) A signal interface, comprising:

an N line bus;

a set of signal lines having N+1 signal lines, where N is an integer;

N+1 transmitters coupled to respective signal lines in the set of signal lines establishing a set of N+1 signal paths with the set of signal lines;

a line maintenance circuit; and

a switch in the N+1 signal paths, and control logic for the switch, which selectively routes N signal paths in the set from the N line bus to N signal lines in the set of signal lines, and routes signal path (n) in the set from the line maintenance circuit to signal line (n) in the set of signal lines, where (n) is changed according to a pattern to selectively perform maintenance on signal paths in the set of N+1 signal paths while enabling data flow on N signal paths in the set from the N line bus; wherein for a change of (n) by switching a first particular signal path from routing to the line maintenance circuit to routing to a line in the N line bus, and a second particular signal path from routing to the line in the N line bus to the line maintenance circuit, the control logic

controls the switch so that transmission of data from the line in the N line bus is uninterrupted.

14. (Original) The signal interface of claim 13, wherein the pattern comprises a periodic pattern.

15. (Original) The signal interface of claim 13, wherein the set of N+1 signal paths includes signal paths logically identified as paths 0 to N, and the pattern comprises a repeating pattern beginning with (n) equal to 0 and increasing to (n) equal to N, and then decreasing to (n) equal to 0.

16. (Original) The signal interface of claim 13, wherein the line maintenance circuit comprises a calibration signal source that produces a signal pattern adapted for calibration of receive clock signals.

17. (Original) The signal interface of claim 13, wherein the line maintenance circuit comprises a calibration signal source that produces a pseudo random signal pattern adapted for calibration of receive clock signals.

18. (Currently Amended) A signal interface, comprising:

an N line bus;

a set of signal lines having N+1 signal lines, where N is an integer;

N+1 transmitters coupled to respective signal lines in the set of signal lines establishing a set of N+1 signal paths with the set of signal lines;

a line maintenance circuit; and

a switch in the N+1 signal paths, and control logic for the switch, which selectively routes N signal paths in the set from the N line bus to N signal lines in the set of signal lines, and routes signal path (n) in the set from the line maintenance circuit to signal line (n) in the set of signal lines, where (n) is changed according to a pattern to selectively perform maintenance on signal paths in the set of N+1 signal paths while enabling data flow on N signal paths in the set from the N line bus ~~The signal interface~~

~~of claim 13~~, wherein ~~the control logic controls the switch~~ for a change of (n) by switching a first particular signal path from routing from the line maintenance circuit to routing to a line in the N line bus, and a second particular signal path from routing to the line in the N line bus from the line maintenance circuit, the control logic controls the switch so that during a settling interval, the first and second particular signal paths both carry data ~~are routed together~~ to the line in the N line bus, and then after the settling interval the second particular signal path is coupled to the line maintenance circuit.

19. (Original) The signal interface of claim 13, wherein the control logic includes logic for coordinating the pattern with a destination of data for the N line bus.

20. (Original) The signal interface of claim 13, wherein said N+1 transmitters, said N line bus, said line maintenance circuit; and said switch comprise components of a single integrated circuit.

21. (Original) The signal interface of claim 13, including logic to power down the N+1 transmitters while continuing to selectively perform maintenance on signal paths in the set of N+1 signal paths.

22. (Original) The signal interface of claim 13, wherein the N+1 transmitters are adapted to transmit data with a data rate higher than 100 MegaHertz.

23. (Original) The signal interface of claim 13, wherein said N+1 transmitters, said N line bus, said line maintenance circuit; and said switch comprise components of a single integrated circuit, and the N+1 transmitters are adapted to transmit data with a data rate higher than 100 MegaHertz to a destination external to the integrated circuit.

24. (Original) The signal interface of claim 13, further including an additional signal line adapted to transmit a source synchronous clock.

25. (Currently Amended) A communication system for inter-chip signals, comprising:

a first integrated circuit, a second integrated circuit, and a set of N+1 communications lines between the first and second integrated circuits;

the first integrated circuit comprising

a first N line bus, where N is an integer;

a set of transmitter signal lines having N+1 transmitter signal lines coupled to respective communications lines in the set of N+1 communications lines;

N+1 transmitters coupled to respective transmitter signal lines in the set of transmitter signal lines establishing a set of N+1 transmitter signal paths with the set of transmitter signal lines;

a calibration signal source; and

a switch in the N+1 transmitter signal paths, and first control logic ~~for the switch,~~ which selectively routes N transmitter signal paths in the set from the first N line bus to N transmitter signal lines in the set of signal lines, and routes transmitter signal path (n) in the set from the calibration signal source to one transmitter signal line in the set of transmitter signal lines, where (n) is changed according to a pattern to selectively supply calibration signals on communication lines in the set of N+1 communication lines while enabling data flow on N communication lines in the set from the first N line bus; and

the second integrated circuit comprising

a set of receiver signal lines having N+1 receiver signal lines coupled to respective communications lines in the set of N+1 communications lines;

N+1 receivers coupled to respective receiver signal lines in the set of receiver signal lines establishing a set of N+1 receiver signal paths with the set of receiver signal lines;

a second N line bus;

a calibration circuit; and

a switch in the N+1 receiver signal paths, and second control logic ~~for the switch~~, which selectively routes N receiver signal paths in the set to the second N line bus and receiver signal path (n) in the set to the calibration circuit, where (n) is changed

according to the pattern to selectively calibrate receiver signal paths in the set of N+1 receiver signal paths while enabling data flow on N receiver signal paths in the set to the second N line bus; and

control logic on at least one of the first and second integrated circuits; wherein for a change of (n) by switching a first particular signal path from routing between the calibration signal source and the calibration circuit to routing to between lines in the first and second N line buses, and a second particular signal path from routing between lines in the first and second N line buses to routing between the calibration signal source and the calibration circuit, the control logic controls the switch so that transmission of data from between the lines in the first and second N line buses is uninterrupted.

26. (Original) The communication system of claim 25, wherein the pattern comprises a periodic pattern.

27. (Original) The communication system of claim 25, wherein the set of N+1 receiver signal paths includes receiver signal paths logically identified as paths 0 to N, and the pattern comprises a repeating pattern beginning with (n) equal to 0 and increasing to (n) equal to N, and then decreasing to (n) equal to 0.

28. (Original) The communication system of claim 25, wherein the calibration signal source produces a signal pattern adapted for calibration of receive clock signals.

29. (Original) The communication system of claim 25, wherein the calibration signal source produces a pseudo random signal pattern adapted for calibration of receive clock signals.

30. (Currently Amended) A communication system for inter-chip signals, comprising:

a first integrated circuit, a second integrated circuit, and a set of N+1 communications lines between the first and second integrated circuits;

the first integrated circuit comprising:

a first N line bus, where N is an integer;

a set of transmitter signal lines having N+1 transmitter signal lines coupled to respective communications lines in the set of N+1 communications lines;

N+1 transmitters coupled to respective transmitter signal lines in the set of transmitter signal lines establishing a set of N+1 transmitter signal paths with the set of transmitter signal lines;

a calibration signal source; and

a switch in the N+1 transmitter signal paths, and first control logic ~~for the switch,~~ which selectively routes N transmitter signal paths in the set from the first N line bus to N transmitter signal lines in the set of signal lines, and routes transmitter signal path (n) in the set from the calibration signal source to one transmitter signal line in the set of transmitter signal lines, where (n) is changed according to a pattern to selectively supply calibration signals on communication lines in the set of N+1 communication lines while enabling data flow on N communication lines in the set from the first N line bus; and

the second integrated circuit comprising:

a set of receiver signal lines having N+1 receiver signal lines coupled to respective communications lines in the set of N+1 communications lines;

N+1 receivers coupled to respective receiver signal lines in the set of receiver signal lines establishing a set of N+1 receiver signal paths with the set of receiver signal lines;

a second N line bus;

a calibration circuit; and

a switch in the N+1 receiver signal paths, and second control logic ~~for the switch~~, which selectively routes N receiver signal paths in the set to the second N line bus and receiver signal path (n) in the set to the calibration circuit, where (n) is changed according to the pattern to selectively calibrate receiver signal paths in the set of N+1 receiver signal paths while enabling data flow on N receiver signal paths in the set to the second N line bus; and

wherein ~~The communication system of claim 25, wherein the first control logic controls the switch~~ for a change of (n) by switching a first particular transmitter signal

path from routing from the calibration signal source to routing from a line in the first N line bus, and a second particular transmitter signal path from routing from the line in the first N line bus to routing from the calibration signal source, the first control logic controls the switch in the N+1 transmitter signal paths so that during a settling interval, the first and second particular transmitter signal paths both carry data ~~are routed together~~ from the line in the first N line bus, and then after the settling interval the second particular signal path is routed from the calibration signal source.

31. (Currently Amended) The communication system of claim 30 ~~25~~, wherein ~~the first control logic controls the switch~~ for a change of (n) by switching a first particular receiver signal path from routing to the calibration circuit to routing to a line in the second N line bus, and a second particular receiver signal path from routing to the line in the second N line bus to the calibration circuit, the second control logic controls the switch in the N+1 receiver signal paths so that during a settling interval, the first and second particular receiver signal paths both carry data for ~~are routed together to~~ the line in the second N line bus, and then after the settling interval the second particular receiver signal path is coupled to the calibration circuit.

32. (Original) The communication system of claim 25, wherein the first control logic and second control logic include logic for coordinating the pattern.

33. (Original) The communication system of claim 25, including logic to power down the N+1 transmitters while continuing to selectively supply calibration signals on transmitter signal paths in the set of N+1 transmitter signal paths.

34. (Original) The communication system of claim 25, including logic to power down the N+1 receivers while continuing to selectively calibrate receiver signal paths in the set of N+1 receiver signal paths.

35. (Original) The communication system of claim 25, wherein the N+1 transmitters and the N+1 receivers are adapted to communicate via the set of communications lines with a data rate higher than 100 MegaHertz.

36. (Original) The communication system of claim 25, further including an additional communication line adapted for a source synchronous clock.

37. (Original) A method for managing a high speed communication interface for a parallel bus having N bus lines, where N is an integer, comprising:

establishing N+1 communication lines;

performing a maintenance operation on communication line (n) of the N+1 communications lines and enabling paths from the N bus lines on N of the N+1 communications lines;

after performing the maintenance operation on communication line (n) of the N+1 communications lines, changing (n) and performing a maintenance operation a next communication line of the N+1 communication lines.

38. (Currently Amended) The method of claim 37, wherein performing the maintenance operation includes:

transmitting a calibration signal on the communication line (n) from a calibration signal source;

receiving the calibration signal on the communication line (n) of the N+1 communications lines; and

calibrating a parameter associated with the communication line (n) on the N+1 communications lines in response to the calibration signal.

39. (Currently Amended) The method of claim 37, including transmitting data from the N bus lines while performing the maintenance operation on the communication line (n).

40. (Currently Amended) The method of claim 37, including entering a reduced power consumption state on at least one of receivers and transmitters on the N of the communication lines, while performing the maintenance operation on the communication line (n).

41. (Original) The method of claim 37, for a changing (n) to switch a first particular communication line from subject of the maintenance operation to communicating from a line on the N line bus, and a second particular communication line from communicating from the line on the N line bus to subject of the maintenance operation, routing the first and second particular communication lines together from the line in the N line bus during a settling interval, and then after the settling interval performing the maintenance operation on the second particular communication line.

42. (Original) The method of claim 37, including changing (n) according to a continuous periodic pattern.

43. (Original) The method of claim 37, wherein the set of N+1 communication lines includes communication lines logically identified as paths 0 to N, and including changing (n) according to a repeating pattern beginning with (n) equal to 0 and increasing to (n) equal to N, and then decreasing to (n) equal to 0.

44. (Currently Amended) The method of claim 37, wherein performing the maintenance operation includes sending a calibration signal from a source on the communication line (n), the calibration signal comprising a signal pattern adapted for calibration of receive clock signals.

45. (Currently Amended) The method of claim 37, wherein performing the maintenance operation includes sending a calibration signal from a source on the communication line (n), the calibration signal comprising a pseudo random signal pattern adapted for calibration of receive clock signals.

46. (Original) The method of claim 37, further including providing a source synchronous clock.

47. (Original) A signal interface, comprising:

a set of signal lines;

a set of receivers coupled to respective signal lines in the set of signal lines;

a bus comprising a set of bus lines;

a line maintenance circuit; and

a switch coupled to the set of receivers, to the bus and to the line maintenance circuit, and control logic for the switch, which selectively routes signals in parallel from receivers in the set of receivers to bus lines in the set of bus lines and to the line maintenance circuit, where the receiver in the set of receivers routed to the line maintenance circuit is changed according to a pattern to selectively maintain signal paths over said set of signal lines without interrupting data flow from the set of receivers from the set of signal lines.

48. (Currently Amended) A transmission circuit on an integrated circuit, comprising:

a line maintenance circuit to output a line maintenance signal;

a set of transmitters coupled to receive a first set of signals and the line maintenance signal, and to output a second set of signals, wherein the second set of signals includes the first set of signals and the maintenance signal; and

a switch coupled to the set of transmitters and a control logic for the switch, to selectively route the first set of signals and the line maintenance signal in parallel to the set of transmitters, where the transmitter in the set of transmitters routed to [by] the line maintenance circuit is changed according to a pattern to selectively maintain the second set of signals from the set of transmitters and to permit the maintenance signal to be used as a calibration signal, the transmitter in the set of transmitters routed to the line maintenance circuit is changed without interruption of transmission of the first set of signals.

49. (Currently Amended) A receiver circuit on an integrated circuit, comprising:

means for receiving a first set of signals and a line maintenance signal, and to output a second set of signals;

means for calibrating the means for receiving without interrupting the outputting of the second set of signals, the means for calibrating coupled to receive the line maintenance signal;

means for routing the first set of signals and the line maintenance signal in parallel from the means for receiving, wherein the routing changes according to a pattern to selectively maintain the second set of signals and to permit the maintenance signal to be used as a maintenance signal for maintaining different portions of the means for receiving.

50. (New) A signal interface, comprising:

a set of signal lines having N+1 signal lines, where N is an integer;

N+1 receivers coupled to respective signal lines in the set of signal lines establishing a set of N+1 signal paths with the set of signal lines;

an N line bus;

a line maintenance circuit; and

a switch in the N+1 signal paths, and control logic for the switch, which selectively routes N signal paths in the set to the N line bus and signal path (n) in the set to the line maintenance circuit, where (n) is changed according to a pattern to selectively maintain signal paths in the set of N+1 signal paths while enabling data flow on N signal paths in the set to the N line bus; wherein the line maintenance circuit performs calibration of the receiver coupled to signal path (n) routed to the line maintenance circuit, independent of the data flow on the N line bus.

51. (New) A signal interface, comprising:

an N line bus;

a set of signal lines having N+1 signal lines, where N is an integer;

N+1 transmitters coupled to respective signal lines in the set of signal lines establishing a set of N+1 signal paths with the set of signal lines;

a line maintenance circuit; and

a switch in the N+1 signal paths, and control logic for the switch, which selectively routes N signal paths in the set from the N line bus to N signal lines in the set of signal lines, and routes signal path (n) in the set from the line maintenance circuit to signal line (n) in the set of signal lines, where (n) is changed according to a pattern to selectively perform maintenance on signal paths in the set of N+1 signal paths while enabling data flow on N signal paths in the set from the N line bus, independent of the data flow on the N line bus.

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